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09/854,349	05/11/2001	Youichi Imamura	P1500D1.R	8679

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EXAMINER

BELL, PAUL A

ART UNIT	PAPER NUMBER
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2675

DATE MAILED: 01/16/2002

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Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/854,349

Applicant(s)

IMAMURA

Examiner

Paul Bell

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– The MAILING DATE of this communication appears on the cover sheet with the correspondence address –

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

1) ☒ Responsive to communication(s) filed on May 11, 2001

2a) ☐ This action is FINAL.

2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 35 C.D. 11; 453 O.G. 213.

## Disposition of Claims

4) ☒ Claim(s) 1-16 is/are pending in the application.

4a) Of the above, claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.

6) ☒ Claim(s) 1-16 is/are rejected.

7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.

8) ☐ Claims \_\_\_\_\_ are subject to restriction and/or election requirements.

## Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are objected to by the Examiner.

11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved.

12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. § 119

13) ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a) ☒ All b) ☐ Some\* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.

3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

## Attachment(s)

15) ☒ Notice of References Cited (PTO-892)

18) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_

16) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)

19) ☐ Notice of Informal Patent Application (PTO-152)

17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). 3

20) ☐ Other: \_\_\_\_\_

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## DETAILED ACTION

### *Claim Rejections - 35 USC § 112*

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:  
The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.
2. Claims 7-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With regard to claim 7 it recites “a device” on line 9 and again in line 15, this format is considered indefinite because it is not clear as to if applicant is claiming a “second” device in line 15 or is referring back to the or said device in line 9.

With further regard to claim 7 it recites “a display device” on line 12 and again in line 19, this format is considered indefinite because it is not clear as to if applicant is claiming a “second” display device in line 19 or is referring back to the or said display device in line 12.

With regard to claim 8 it recites “a device” on line 9 and again in line 16, this format is considered indefinite because it is not clear as to if applicant is claiming a “second” device in line 16 or is referring back to the or said device in line 9.

With further regard to claim 8 it recites “a display device” on line 12 and again in line 20, this format is considered indefinite because it is not clear as to if applicant is claiming a “second” display device in line 20 or is referring back to the or said display device in line 12.

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With regard to claim 9 it recites "a display device" on line 11 and again in line 16, this format is considered indefinite because it is not clear as to if applicant is claiming a "second" display device in line 16 or is referring back to the or said display device in line 11.

With regard to claim 10 it recites "a display device" on line 11 and again in line 17, this format is considered indefinite because it is not clear as to if applicant is claiming a "second" display device in line 17 or is referring back to the or said display device in line 11.

With regard to claim 11 it recites "a display device" on lines 6 and 7 and again in line 11, this format is considered indefinite because it is not clear as to if applicant is claiming a "second" display device in line 11 or is referring back to the or said display device in lines 6 and 7.

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371© of this title before the invention thereof by the applicant for patent.

4. Claims 1-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Inoue et al. (5,952,290).

With regard to claim 1, Inoue et al. discloses a method of controlling a flat display unit (figure 1), comprising a flat display panel driven in accordance with display driving voltages (figure 1, item 11), display driver means for selecting the display driving voltages supplied to the flat display panel (figure 1, comprising items 1, 26, 14, 12 and 13) and a display power source

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circuit (figure 1, POWER CONTROLLER items 15, 1 and Vcc) for supplying the display driving voltages to the display driver means in response to a power control signal (figure 1, POWER OFF SIGNAL), the method of controlling the flat display unit comprising the steps of: detecting a logic power voltage (figure 1, Vcc, item 1) activating a logic circuit (figure 1, CONTROLLER item 14) of the flat display unit by the display driver means; supplying the power control signal from the display driver means to the power source circuit (figure 1, items 14 and 15), said power control signal having a delay time after the detection of said logic power voltage (column 11, lines 44-45); supplying the display driving voltages to the display driver means in response to the power control signal by the power source circuit; and selecting the display driving voltages supplied from the power source circuit to the flat display panel by the display driver means (column 4, lines 45-67 and column 5, lines 1-30).

With regard to claim 2 Inoue et al. further comprising the step of supplying a start signal controlling a start of display to the display driver means after supplying the display driving voltages to the display driver means (figure 1, item 1).

With regard to claim 3, Inoue et al. discloses a method of controlling a flat display device comprising a flat display panel module unit (figure 2) and a display control unit for supplying control signals to control display of the flat display panel module unit (figure 2, item 14 CONTROLLER), said flat display panel module unit including a flat display panel driven in accordance with display driving voltages (figure 2, item 11), display driver means for selecting the display driving voltages to the flat display panel (figure 2, comprising items 1, 26, 14, 12 and

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13 ) and a display power source circuit for supplying the display driving voltages to the display driver means (figure 2, Vcc) in response to a power control signal (figure 2, END SIGNAL), the method of controlling the flat display unit comprising the steps of: supplying the power control signal to the power source circuit by the display driver means (figure 2, item 12, END SIGNAL), the power control signal having a delay time after (column 11, lines 44-45) a logic power voltage (figure 2, Vcc, item 1 ) has been supplied to a logic circuit (figure 2, part of item 14 the CONTROLLER ) of the flat display device; supplying the display driving voltages to the display driver means in response to the power control signal by the power source circuit (column 5, lines 26-30); supplying a display start signal (figure 2, item 12, END SIGNAL) controlling a start of the selection of the display driving voltages by the display driver means in response to the control signal supplied from the display control unit, said display start signal having a delay time after the power control signal has supplied to the power source circuit (column 11, lines 44-45 ) and selecting the display driving voltages supplied from the power source circuit to supply to the flat display panel in response to the start signal (column 4, lines 45-67 and column 5, lines 1-30).

With regard to claim 4, Inoue et al. discloses wherein the flat display panel module unit is arranged separately from the display control unit (figure 2, item 11).

With regard to claim 5, Inoue et al. discloses a flat display unit comprising: a flat display panel for being driven in accordance with display driving voltages (figure 1, item 11 ); display driver means for display driving voltages supplied to said flat display panel (figure 1, comprising items 1, 26, 14, 12 and 13 ), said display driver means comprising a logic circuit (figure 1,

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CONTROLLER item 14) and a detection means (figure 1, item 1 ) for detecting a logic power voltage (figure 1, Vcc, item 1) activating said logic circuit and for supplying a power control signal (figure 1, POWER OFF SIGNAL ) having a delay time after (column 11, lines 44-45) the detection of the logic power voltage; and a display power source circuit (figure 1, POWER CONTROLLER items 15, 1 and Vcc ) for supplying the display driving voltages to said display driver means in response to the power control signal.

With regard to claim 6, Inoue et al. discloses a flat display device comprising a flat display panel module unit (figure 2) and a display control unit for supplying control signals to control display of the flat display panel module unit (figure 2, item 14 CONTROLLER), said flat display panel module unit comprising: a flat display panel driven in accordance with display driving voltages (figure 2, item 11); display driver means for selecting the display driving voltages supplied to said flat display panel (figure 2, comprising items 1, 26, 14, 12 and 13 ) and for supplying a power control signal (figure 2, END SIGNAL) having a delay time (column 11, lines 44-45) after a logic power voltage (figure 2, Vcc, item 1 ) has been supplied to a logic circuit of said display driver means; and a display power source circuit for supplying the display driving voltages to said display driving means (figure 2, Vcc) in response to the power control signal, wherein said display driver means starts the selection of the display driving voltages in response to a display start signal having a delay time after the power control signal has supplied to said power source circuit (column 4, lines 45-67 and column 5, lines 1-30).

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With regard to claim 7, Inoue et al. discloses a display control device for controlling a display device driver circuit that drives a display device, and for controlling a display device power circuit that provides power to a display device driver circuit to cause a display on a display device, comprising ( figure 1): a device (figure 1, item 12) that outputs to a display device power circuit (figure 1, Vcc and item 15, POWER CONTROLLER and note Vcc goes into item 14) a signal (figure 1, END SIGNAL) to initiate supply of power to cause a display on a display device (figure 1, item 11), in response to an external display start signal (figure 1, item 14, CONTROL SIGNAL ); and a device (figure 1, item 14) that outputs to a display device driver circuit ( figure 1, items 11 and 12) a signal to initiate output of a drive signal from the display device driver circuit to a display device (figure 1, item 14, CONTROL SIGNAL or ERASE SIGNAL or SCAN LINE ADDRESS SIGNAL) , after a first period of time has elapsed following output of the signal to initiate supply of power (column 5, lines 27-30).

With regard to claim 8, Inoue et al. discloses a display control device for controlling a display device driver circuit that drives a display device, and for controlling a display device power circuit that provides power to a display device driver circuit to cause a display on a display device, comprising: a device (figure 1, item 12) that outputs to a display power circuit (figure 1, Vcc and item 15, POWER CONTROLLER and note Vcc goes into item 14 ) a signal (figure 1, END SIGNAL) to initiate supply of power to cause a display on a display device ( figure 1, item 11), after a first period of time has elapsed following input of an external display start signal (figure 1, item 14, CONTROL SIGNAL ); and a device ( figure 1, item 14) that outputs to a



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display device driver circuit (figure 1, items 11 and 12) a signal to initiate output of a drive signal from the display device driver circuit to a display device, after a second period of time has elapsed following output of said signal to initiate supply of power (column 5, lines 27-30).

With regard to claim 9, Inoue et al. discloses a display control apparatus comprising: a display control device (figure 1, item 14) to control a display device power circuit (figure 1, item 15 and Vcc) that provides power to cause a display on a display device, comprising: a device (figure 1, END SIGNAL) that outputs to a display device power circuit a signal to initiate supply of power to cause a display on a display device, in response to an external display start signal (figure 1, CONTROL SIGNAL); and a display device driver circuit that initiates output of a drive signal to a display device (figure 1, item 12), after a first period of time has elapsed following output of said signal to initiate supply of power (column 5, lines 27-30).

With regard to claim 10, Inoue et al. discloses a display control apparatus comprising: a display control device (figure 2, item 14) to control a display device power circuit (figure 2, Vcc) that provides power to cause a display on a display device (figure 2, item 11), comprising a device (figure 2, item 12) that outputs to a display device power circuit a signal to initiate supply of power to cause a display on a display device, after a first period of time has elapsed following input of an external display start signal (figure 2, item 2); and a display device driver circuit that initiates output of a drive signal to a display device (figure 2, item 12), after a second period of time has elapsed following output of said signal to initiate supply of power (column 5, lines 27-30).

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With regard to claim 11, Inoue et al. discloses a display control apparatus for driving a display device, comprising: a display device power circuit (figure 2, Vcc) that initiates supply of power to cause a display on a display device (figure 2, item 11), in response to an external display start signal (figure 2, item 2); and a display device driver circuit that initiates output of a drive signal to a display device (figure 2, item 2) after a first period of time has elapsed following the initiation of supply of power (column 5, lines 27-30).

With regard to claim 12, Inoue et al. discloses a display control apparatus for driving a display device, comprising: a display device power circuit (figure 2, Vcc) that initiates supply of power to cause a display on a display device (figure 2, item 11) after a first period of time has elapsed following input of an external display start signal (figure 2, item 2); and a display device driver circuit that initiates output of a drive signal to said display device (figure 2, item 12) after a second period of time has elapsed following the initiation of supply of power (column 5, lines 27-30).

With regard to claim 13, Inoue et al. discloses a method of controlling a display apparatus comprising a display control device (figure 2, item 14), a display device that is driven by a display driving voltage (figure 2, item 11), a display device driver unit that selects the display driving voltage that is to be supplied to the display device (figure 2, item 12), and a display device power supply (figure 2, Vcc) that supplies the display driving voltage to the display device driver unit in response to a power control signal (figure 2, CONTROL SIGNAL ), the method comprising: a first step of receiving and processing input of a signal to instruct start of a display on sequence

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(figure 2, item 2 and 26); a second step of supplying the power control signal to control power-on of the display device power supply (figure 2, the signal from item 26 to item 14); a third step of supplying the display driving voltage to the display device driver unit from the display device power supply in response to the power control signal (figure 1, ERASE SIGNAL); a fourth step of supplying to the display device driver unit a start signal to control start of causing a display on the display device (figure 2 SCAN LINE ADDRESS SIGNAL) ; and a fifth step of selecting by the display device driver the display driving voltage that is supplied to the display device (figure 2, DISPLAY DATA).

With regard to claim 14, Inoue et al. discloses wherein the method advances to the first step after a logic voltage has been supplied to the display control device of the display apparatus (figure 2, switch 2).

With regard to claim 15, Inoue et al. discloses 15, wherein the method advances to the fourth step after at least a first delay time has elapsed following the third step (column 5, lines 27-30).

With regard to claim 16, Inoue et al. discloses wherein the method advances to the second step after at least a first delay time has elapsed following the first step (It is inherent that after activating a switch item 2 there is delay in circuit 26 relating to processing and propagation of signal before a signal is sent to item 14).

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5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul Bell whose telephone number is (703) 306-3019. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Saras, can be reached at (703) 305-9720.

Any response to this action should be mailed to: Commissioner of Patents and Trademarks  
Washington, D.C. 20231  
or faxed to: (703) 872-9314

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist). Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

*Paul Bell*  
Paul Bell  
Art unit 2675  
11 January 2002

*Steven Saras*  
STEVEN SARAS  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2600